PTO-1449 to include "pp. 782-785" for the Furue article. As a courtesy to the Examiner, the Applicants have attached a corrected Form PTO-1449. The Applicants respectfully request that the Examiner provide an initialed copy of the corrected Form PTO-1449 to effectuate entry of the correction.

Claims 1-17, 19-30 and 47-58 are pending in the present application, of which claims 1-12, 19, 20, 47 and 48 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

Applicants appreciate the Examiner's time in conducting a personal interview with the undersigned in the subject application on April 5, 2005. During the interview, the outstanding rejection based on JP 07-038113 to Morosawa was discussed. More specifically, it was submitted by Applicant that the machine generated translation provided by the USPTO, which is currently of record, contains translational errors that result in the translation being confusing and inaccurate. Applicant presented a partial translation of what is believed to be the most relevant portions of Morosawa for discussion during the interview and agreed to submit a full translation for consideration by the Examiner with this response. As described in more detail below, such full translation is attached and believed to support Applicant's arguments during the interview that Morosawa fails to disclose or suggest a leveling step by heating after removal of a natural oxidation film as claimed.

Paragraph 3 of the Official Action rejects claims 47, 48 and 53-58 as anticipated by JP 07-038113 to Morosawa. The Applicants respectfully traverse the rejection because the Official Action has not established an anticipation rejection.

As stated in MPEP § 2131, to establish an anticipation rejection, each and every element as set forth in the claim must be described either expressly or inherently in a single prior art reference. Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

The Applicants respectfully submit that an anticipation rejection cannot be maintained against the independent claims of the present application. Morosawa does not teach all the elements of the independent claims, either explicitly or inherently. The independent claims recite leveling a surface of a semiconductor film by heating after removing a natural oxidation film or an oxide film or after treatment with a hydrofluoric acid. Specifically, independent claims 1 and 47 recite leveling the surface of the semiconductor film by heating after removing said natural oxidation film; independent claims 2 and 5 recite leveling the surface of the semiconductor film by heating in a reducing atmosphere after removing said oxide film; independent claims 3 and 6 recite leveling the surface of the semiconductor film by heating in an inert gas after removing said oxide film; independent claims 4 and 19 recite leveling the surface of the semiconductor film by heating in an atmosphere after removing said oxide film; and independent claims 7-12, 20 and 48 recite leveling the surface of the semiconductor film by heating after the treatment with said hydrofluoric acid.

The Official Action broadly asserts that Morosawa teaches, for example with respect to claim 47, "leveling the surface of the semiconductor film by heating in inert gas (i.e., nitrogen gas) or in reducing atmosphere (i.e., in hydrogen) after the treatment with the hydrofluoric acid" (page 3, Paper No. 20041210). The Official Action makes similar assertions in the Response to Arguments beginning on page 34.

As noted during the interview, the <u>machine generated translation</u> of Morosawa of record states, in relevant part:

> [0010] Next, if it heat-treats at the temperature of about 500 degrees C in nitrogen-gas-atmosphere mind in order to stabilize the membraneous quality of the polish recon thin film 6, as shown in drawing 4(A), the natural oxidation film 8 will be formed in the front face of the polish recon thin film 6. Next, it etches by dipping in fluoric acid a grade for 1 minute 1%. Then, the natural oxidation film 8 is removed by several second about room, and about 100A of surface layers of the polish recon thin film 6 is removed after this. This condition is shown in drawing 4(B). Thus, since about 100A of surface layers of the polish recon thin film 6 is removed, the impurity 7 which focused on the surface layer of the polish recon thin film 6, and remains will also be removed by coincidence. <u>In addition, in order</u>

to stabilize the membraneous quality of the polish recon thin film 6, you may heat-treat at the temperature of about 500-600 degrees C not in nitrogen-gas-atmosphere mind but in an oxygen ambient atmosphere. In this case, since etching time can be shortened rather than the case of heat treatment in nitrogen-gas-atmosphere mind, the damage given to a glass substrate 1 can be lessened. Moreover, etching may be dry etching. (Emphasis added)

During the interview it was asserted that the emphasized portion of Morosawa was being relied upon to teach a second heat treatment occurring after the removal of the natural oxide film. However, as stressed during the interview, it is respectfully submitted that this portion of Morosawa does not disclose or suggest a second heat treatment step, but rather discloses an alternative to the heat treatment previously disclosed in the first sentence of paragraph [0010]. It is noted that this paragraph is replete with obvious translational errors and during the interview the following, more accurate translation of this portion was presented:

> [0010] Next, heat treatment is conducted at approximately 500 °C in a nitrogen gas atmosphere in order to stabilize the membraneous quality of the poly-silicon thin film 6. Then, as shown in FIG. 4A, a natural oxidation film 8 is formed on a surface of the poly-silicon thin film 6. Next, etching is performed by dipping in 1% of fluoric acid for approximately 1 minute. Then, the natural oxidation film 8 is removed in several seconds, and approximately 100 angstrom of surface layer of the poly-silicon thin film 6 is removed after this. This condition is shown in FIG. 4B. Thus, since approximately 100 angstrom of a surface layer of the poly-silicon thin film 6 is removed, the impurity 7 which is concentrated and remains at the surface layer of the poly-silicon thin film 6 is also removed at the same time. Furthermore, in order to stabilize the membraneous quality of the poly-silicon thin film 6, the heat treatment may be conducted at a temperature of approximately 500 to 600 °C in an oxygen gas atmosphere instead of the nitrogen gas atmosphere. In this case, since etching time can be shorter than the case of heat treatment in the nitrogen gas atmosphere, a damage given to the glass substrate 1 can be lessened. Moreover, etching may be dry etching. (Emphasis added)

It is respectfully submitted that the underlined portion of the above translation can clearly only be properly interpreted to present an alternative to the first heat treatment

step that occurs prior to the removal of the native oxide film. Both the underlined portion and the first sentence of the paragraph make reference to stabilizing the membraneous quality of the film (i.e. both have the same intended purpose) and the emphasized portion makes clear that "the heat treatment may be conducted at a temperature of approximately 500 to 600 °C in an oxygen gas atmosphere instead of the nitrogen gas atmosphere." By referring to the use of an oxygen gas atmosphere for the heat treatment (i.e. the same, previously discussed heat treatment) instead of (i.e. as a replacement for) the nitrogen gas atmosphere, it is clear that the only fair interpretation of Morosawa is that this step is an alternative, or replacement, for the previously mentioned heat treatment step and not intended as a second, additional, heat treatment step.

It is further noted that the subsequent portions of paragraph 10 make reference to advantages achieved by the oxygen atmosphere heat treatment as compared to the nitrogen atmosphere heat treatment, which include shorter etching time. It is respectfully submitted that this further supports the proposition that this is a replacement for the earlier heat treatment step in that the statement immediately following the first disclosure of the nitrogen atmosphere heat treatment discusses that "etching is performed by dipping in 1% of fluoric acid for approximately 1 minute. Then, the natural oxidation film 8 is removed in several seconds." Thus, by reference to the shorter etching time achieved using the oxygen atmosphere as compared to a nitrogen atmosphere, it is clear that this heat treatment in oxygen is intended to replace the earlier nitrogen gas heat treatment step.

Since Morosawa does not teach all the elements of the independent claims, either explicitly or inherently, an anticipation rejection cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 102 are in order and respectfully requested.

Paragraph 5 of the Official Action rejects claims 19, 20, 23-30, 51 and 52 as obvious based on Morosawa. Paragraph 6 of the Official Action rejects claims 21, 22,

49 and 50 as obvious based on the combination of Morosawa and U.S. Patent No. 5,608,232 to Yamazaki et al. Paragraph 7 of the Official Action rejects claims 1-12 and 14-17 as obvious based on the combination of Morosawa and JP 09-186336 to Kudo et al. Paragraph 8 of the Official Action rejects claim 13 as obvious based on the combination of Morosawa, Kudo and Yamazaki. The Applicants respectfully traverse the rejection because the Official Action has not made a *prima facie* case of obviousness.

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The prior art, either alone or in combination, does not teach or suggest leveling a surface of a semiconductor film by heating after removing a natural oxidation film or an oxide film or after treatment with a hydrofluoric acid. Morosawa, Kudo and Yamazaki, either alone or in combination, do not teach or suggest at least the above-referenced features of the present invention. As noted above, Morosawa fails to teach leveling a

surface of a semiconductor film by heating after removing a natural oxidation film or an oxide film or after treatment with a hydrofluoric acid. Kudo and Yamazaki do not cure the deficiencies in Morosawa. Kudo is relied upon to allegedly teach irradiating an amorphous silicon film with an excimer laser in an atmosphere containing air (i.e. page 14, Paper No. 20040616) and Yamazaki is relied upon to allegedly teach furnace annealing (i.e. page 11, Id.). However, Morosawa, Kudo and Yamazaki, either alone or in combination, do not teach or suggest leveling a surface of a semiconductor film by heating after removing a natural oxidation film or an oxide film or after treatment with a hydrofluoric acid.

Since Morosawa, Kudo and Yamazaki do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
BK		JP	07-130652			05/19/1995	—	AB

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
BK		R. Shimokawa et al., *Characterization of High-Efficiency Cast-Si Solar Cell Wafers by MBIC Measurement*, Japanese Journal of Applied Physics, Volume 27, No. 5, May, 1988, pp. 751-758	
BK		H. Furue et al., *P-78: Characteristics and Driving Scheme of Polymer-Stabilized Monostable FLCD Exhibiting Fast Response Time and High Contrast Ratio with Gray-Scale Capability*, SID, 1998, pp. 782-785.	
BK		T. Yoshida, *33.2: A Full-Color Thresholdless Antiferroelectric LCD Exhibiting Wide Viewing Angle with Fast Response Time*, SID Digest, 1997, pp. 841-844.	
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Examiner Signature	Biruk Kebede	Date Considered	12/10/2004

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(54) [Title of the Invention] MANUFACTURING METHOD OF THIN FILM TRANSISTOR

(57) [Abstract]

[Object] To enhance membraneous quality of a poly-silicon thin film.

[Structure] An amorphous silicon thin film is formed over a top surface of a glass substrate 1 to have a thickness that is thicker by about 100 angstrom than a thickness to be designed. Then, the amorphous silicon thin film is polymerized by excimer laser

exposure to become a poly-silicon thin film 6. Then, heat treatment is conducted in a nitrogen gas atmosphere to stabilize membraneous quality of the poly-silicon thin film 6 and then a natural oxidation film 8 is formed on the surface of the poly-silicon thin film 6. Then, etching is performed by dipping in 1% of fluoric acid for approximately 1 minute. Then, the natural oxidation film 8 is removed in several seconds, and approximately 100 angstrom of the surface layer of the poly-silicon thin film 6 is removed after this. Thus, the amorphous silicon thin film melted by laser annealing solidifies to be polymerized from the glass substrate 1 side, and if an impurity 7 existing in the amorphous silicon thin film is concentrated and remains at the surface layer of the poly-silicon thin film 6, the remaining impurity 7 is removed.

[Scope of Claims]

[Claim 1] A manufacturing method of a thin film transistor, characterized in that after a semiconductor thin film formed over a substrate is annealed by a laser, a surface layer of the semiconductor thin film is removed together with impurities concentrated at the surface layer.

[Claim 2] The manufacturing method of a thin film transistor as recited in Claim 1, characterized in that the semiconductor thin film is an amorphous silicon thin film before the laser annealing is conducted, and the amorphous silicon thin film is polymerized by the laser annealing.

[Claim 3] The manufacturing method of a thin film transistor as recited in Claim 1, characterized in that heat treatment is conducted after the laser annealing and the surface layer of the semiconductor thin film is removed after this.

[Claim 4] The manufacturing method of a thin film transistor as recited in Claim 3, characterized in that the heat treatment is conducted in a nitrogen gas atmosphere.

[Claim 5] The manufacturing method of a thin film transistor as recited in Claim 3, characterized in that the heat treatment is conducted in an oxygen gas atmosphere.

[Detailed Description of the Invention]

[0001]

[Industrial Field of the Invention] The present invention relates to a manufacturing method of a thin film transistor.

[0002]

[Prior Art] In a manufacturing field of a thin film transistor, there is a case that an amorphous silicon thin film formed over a glass substrate is annealed by a laser to be polymerized for obtaining a poly-silicon thin film. In this case, the amorphous silicon thin film melted by laser annealing solidifies to be polymerized from the glass substrate side. Further, there is a case that a poly-silicon thin film into which ions have been implanted is activated by laser annealing. Also in this case, the poly-silicon thin film melted by laser annealing solidifies from the glass substrate side.

[0003]

[Problems to be solved by the Invention] As described above, a semiconductor thin film made of an amorphous silicon thin film or the like melted by laser annealing solidifies from the glass substrate side. Thus, impurities existing in the semiconductor thin film are concentrated at a surface layer thereof and remain. As the result thereof, in a thin film transistor provided with a semiconductor thin film having such a structure, there are problems in that membraneous quality of the semiconductor thin film is not favorable, and electric characteristics such as on-current, off-current and a threshold voltage are deteriorated. An object of this invention is to provide a manufacturing method of a thin film transistor that can enhance membraneous quality of a semiconductor thin film.

[0004]

[Means for solving the Problems] According to this invention, after a semiconductor thin film formed over a glass substrate is annealed by a laser, a surface layer of the semiconductor thin film and impurities concentrated at the surface layer are removed together.

[0005]

[Operation] According to this invention, membraneous quality of the semiconductor thin film can be enhanced by removing the surface layer of the semiconductor thin film together with impurities concentrated at the surface layer.

[0006]

[Example] Each of FIGS. 1 to 8 shows each manufacturing step of a thin film transistor in one example of this invention. Then, a manufacturing method of a thin film transistor is described sequentially with reference to these drawings.

[0007] First, as shown in FIG. 1, a hydrogenated amorphous silicon thin film 2 is deposited by plasma CVD using a mixed gas of SiH_4 and H_2 over a top surface of a glass substrate 1. In this case, the film-thickness of the hydrogenated amorphous silicon thin film 2 is set somewhat thicker than a thickness to be designed. For example, if the thickness to be designed is about 500 angstrom, the film-thickness is set about 600 angstrom by adding 100 angstrom. In addition, as the condition of deposition, the temperature of the glass substrate 1 is about 200 to 350 °C, preferably about 250 °C, and a mixed gas of SiH_4 of about 10 to 20 SCCM and H_2 of about ten times thereof is used. Then, the hydrogen content of the hydrogenated amorphous silicon thin film 2 is about 10 to 20 atomic%. Then, dehydrogenation treatment is conducted to prevent hydrogen from boiling rapidly to cause defects when high energy is added by excimer laser exposure in a subsequent step. In this case, heat treatment is conducted for about one hour in a nitrogen gas atmosphere at a temperature of about 450 °C so that the hydrogen content is 3 atomic% or less, preferably 1 atomic% or less.

[0008] Next, as shown in FIG. 2, a photo resist film 4 is formed over a top surface of a portion corresponding to a region except a source-drain formation region 3a of an amorphous silicon thin film 3 that has been dehydrogenated. Then, ions such as a phosphorus ion or a boron ion are implanted into the source/drain formation region 3a of the amorphous silicon thin film 3 using this photo resist film 4 as a mask to form an ion-implanted region 5. Thereafter, the photo resist film 4 is removed.

[0009] Next, as shown in FIG. 3, the amorphous silicon thin film 3 is irradiated with XeCl excimer laser with a wavelength of 308 nm, from 250 to 350 mJ/cm^2 of the energy density, and 50 ns of pulse width. The condition of irradiation is set at the substrate temperature from 200 to 400 °C and in a vacuum. Then, the amorphous silicon thin film 3 is polymerized to be a poly-silicon thin film 6 and the ion-implanted region 5 is activated at the same time. In this case, when the amorphous silicon thin film 3 melted

by laser annealing solidifies from a glass substrate 1 side, an impurity 7 which exists in the amorphous silicon thin film 3 is concentrated at the surface layer of the poly-silicon thin film 6. When temperature of the glass substrate 1 is set at from 200 to 400 degrees C at this time, since a coagulation rate is to be reduced to from 60 to 30% in the case of a room temperature, much more concentration to the surface layer of an impurity can be attained with increase of the diameter of a crystal grain. In addition, of course, excimer laser other than XeCl excimer laser with a wavelength of 308 nm, such as KrF with a wavelength of 248 nm, ArF with a wavelength of 193 nm, ArCl with a wavelength of 175 nm, and XeF with a wavelength of 353 nm, may be used. Moreover, if excimer laser exposure is performed two or more times, the surface layer of an impurity can be concentrated more certainly.

[0010] Next, heat treatment is conducted at approximately 500 °C in a nitrogen gas atmosphere in order to stabilize the membraneous quality of the poly-silicon thin film 6. Then, as shown in FIG. 4A, a natural oxidation film 8 is formed on a surface of the poly-silicon thin film 6. Next, etching is performed by dipping in 1% of fluoric acid for approximately 1 minute. Then, the natural oxidation film 8 is removed in several seconds, and approximately 100 angstrom of surface layer of the poly-silicon thin film 6 is removed after this. This condition is shown in FIG. 4B. Thus, since approximately 100 angstrom of a surface layer of the poly-silicon thin film 6 is removed, the impurity 7 which is concentrated and remains at the surface layer of the poly-silicon thin film 6 is also removed at the same time. Furthermore, in order to stabilize the membraneous quality of the poly-silicon thin film 6, the heat treatment may be conducted at a temperature of approximately 500 to 600 °C in an oxygen gas atmosphere instead of the nitrogen gas atmosphere. In this case, since etching time can be shorter than the case of heat treatment in the nitrogen gas atmosphere, a damage given to the glass substrate 1 can be lessened. Moreover, etching may be dry etching.

[0011] Next, as shown in FIG 5, an unnecessary part of the poly-silicon thin film 6 is removed by element separation. In this condition, the center section of the poly-silicon thin film 6 is set to a channel region 6a, and those opposite sides are set to source/drain regions 6b including an activation ion-implantation region. Next, as shown in FIG. 6, a

gate insulating film 9 which is formed of a silicon oxide film and a silicon nitride film is formed over whole surface of the substrate. That is, the silicon oxide film is first deposited over whole surface of the substrate by sputtering, and subsequently, the silicon nitride film is deposited by plasma CVD using the mixed gas including SiH_4, NH_3, and N_2 on the surface of the silicon oxide film. When the silicon nitride film is deposited by plasma CVD, a temperature of the glass substrate 1 is set at approximately 250 °C, SiH_4 is set at approximately 30 SCCM, NH_3 is set at approximately 60 SCCM, N_2 is set at approximately 390 SCCM and it carries out in output power set at approximately 600 W and a pressure set at approximately 0.5 Torr in order to hydrogenate the poly-silicon thin film 6 at the same time and to reduce dangling bonds thereof. Thus, the gate insulating film 9 is deposited by plasma CVD over the poly-silicon thin film 6 and at the same time, the poly-silicon thin film 6 is hydrogenated to decrease the dangling bonds thereof. Therefore, deposition of the gate insulating film 9 and hydrogenation of the poly-silicon thin film 6 can be performed by one-time plasma CVD at the same time. Consequently, a process only for hydrogenation can be omitted, as a result, the number of manufacturing processes can be lessened. Next, a gate electrode 10 including Cr is formed at the top face of the gate insulating film 9 of the part corresponding to the channel region 6a.

[0012] Subsequently, as shown in FIG. 7, an interlayer insulating film 11 comprising a silicon nitride film is formed over the whole surface. Then, a contact hole 12 is formed in the interlayer insulating film 11 and the gate insulating film 9 of the part corresponding to the source/drain regions 6b. Then, as shown in FIG. 7, source/drain electrodes 13 made of Al to be connected to the source/drain regions 6b through the contact hole 12 are formed by patterning over a top surface of the interlayer insulating film 11. In the thusly obtained field-effect type thin film transistor, it is confirmed that electric characteristics such as on-current, off-current, and a threshold voltage are enhanced, the mobility is 80 $cm^2/V\cdot sec$ or more, and the membraneous quality of the poly-silicon thin film 6 is extremely favorable.

[0013] Note that in the above example, dehydrogenation treatment is conducted after the hydrogenated amorphous silicon thin film 2 is deposited by plasma CVD; however,

without being limited to this, for example, an amorphous silicon thin film without containing hydrogen may be deposited by LPCVD. In this case, the temperature of the glass substrate 1 is about 500 to 600 °C when an amorphous silicon thin film without containing hydrogen is deposited by LPCVD and the energy density of the excimer laser is set at about 400 mJ/cm^2 for polymerization and activation. Therefore, dehydrogenation treatment is not needed in this case. However, since the temperature of the glass substrate 1 is relatively high, about 500 to 600 °C, the increase in the substrate temperature needs more time. In addition, if the temperature of the glass substrate 1 is about 600 °C, a poly-silicon thin film is directly deposited instead of an amorphous silicon thin film, and a crystal grain diameter is grown by excimer laser exposure after that; therefore, a crystal structure of the poly-silicon thin film can be enhanced.

[0014] Further, in the above example, polymerization and activation are conducted at the same time by one-time excimer laser exposure; however, they are conducted separately. The point is that impurities concentrated at the surface layer of the poly-silicon thin film can be removed by laser annealing before forming the gate insulating film 9. At this time, in the case of conducting heat treatment for stabilizing the membraneous quality of the poly-silicon thin film, a natural oxidation film formed on the surface of the poly-silicon thin film is also removed.

[0015] Further, in the above example, the case where this invention is applied to a general thin film transistor having a MOS structure is described. However, this invention can be also applied to a thin film transistor having an LDD structure in which withstand voltage or the like is improved to obtain higher reliability as compared with the general thin film transistor having a MOS structure. For example, in a thin film transistor having an LDD structure shown in FIG. 9 where the same reference numbers are used for portions having the same name as those of FIG. 8, a center section of the poly-silicon thin film 6 is made as a channel region 6a, the opposite sides thereof are source/drain regions 6b having low ion concentration, and the more opposite sides thereof are source/drain regions 6c having high ion concentration. When a thin film transistor having this LDD structure is formed, low concentration of ions are implanted

in a portion for forming the source/drain regions 6b having low ion concentration and the source/drain regions 6c having high ion concentration in the state shown in FIG. 2, for example. Then, the photo resist film 4 is removed, and then a different photo resist film is formed over a top surface of a portion except the portion for forming the source/drain regions 6c having high ion concentration and high concentration of ions may be implanted into the portion for forming the source/drain regions 6c having high ion concentration using the different photo resist film as a mask.

[0016] Moreover, in the above example, the case where this invention is applied to a thin film transistor having a top gate type coplanar structure is described; however, it is clear that this invention can be applied to a thin film transistor having a stagger structure, a back gate type coplanar structure or stagger structure. In the case of a back gate type, a gate electrode and a gate insulating film are formed over a top surface of a glass substrate, an amorphous silicon thin film is deposited thereover, and the amorphous silicon thin film is polymerized to become a poly-silicon thin film. In addition, hydrogenation treatment of the poly-silicon thin film can be conducted at the same time as depositing a passivation film (an insulating film) over the poly-silicon thin film by plasma CVD.

[0017]

[Effect of the Invention] As described above, according to this invention, since a surface layer of a semiconductor thin film is removed together with impurities concentrated at the surface layer, membraneous quality of the semiconductor thin film can be enhanced and electric characteristics such as on-current, off-current, and a threshold voltage can be improved.

[Detailed description of the Drawings]

[FIG. 1] A cross-sectional view of a state where a hydrogenated amorphous silicon thin film is deposited over a top surface of a glass substrate when manufacturing a thin film transistor in one example of this invention.

[FIG. 2] A cross-sectional view of a state where ions are implanted into source/drain formation regions of an amorphous silicon thin film that has been dehydrogenated when manufacturing the thin film transistor.

[FIG. 3] A cross-sectional view of a state where an ion-implanted region is activated at the same time as polymerizing an amorphous silicon thin film by excimer laser exposure when manufacturing the thin film transistor.

[FIG. 4] (A) A cross-sectional view of a state where a natural oxidation film is formed on a surface of the poly-silicon thin film by heat treatment when manufacturing the thin film transistor. (B) A cross-sectional view of a state where the surface layer of the poly-silicon thin film is removed by etching when manufacturing the thin film transistor.

[FIG. 5] A cross-sectional view of a state where an unnecessary part of the poly-silicon thin film is removed by element separation when manufacturing the thin film transistor.

[FIG. 6] A cross-sectional view of a state where a gate insulating film and a gate electrode are formed when manufacturing the thin film transistor.

[FIG. 7] A cross-sectional view of a state where an interlayer insulating film and a contact hole are formed when manufacturing the thin film transistor.

[FIG. 8] A cross-sectional view of a state where source/drain electrodes are formed when manufacturing the thin film transistor.

[FIG. 9] The same cross-sectional view as that of FIG. 8, in the case where this invention is applied to a thin film transistor having an LDD structure.

[Description of Reference Number]

1 glass substrate

3 amorphous silicon thin film

6 poly-silicon thin film

7 impurity

8 natural oxidation film

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Section showing technique